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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/674,215 | 09/29/2003 | Mark Hennecken | 2002-155-TAP | 2514 |

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| EXAMINER | |
|---|---|
| LAMARRE, GUY J | |

| ART UNIT | PAPER NUMBER |
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/674,215 | HENNECKEN ET AL. | |
| | Examiner | Art Unit | |
| | Guy J. Lamarre | 2112 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *29 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/29/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

* Pursuant to 35 USC 131, **Claims 1-18** are presented for examination.

### Abstract

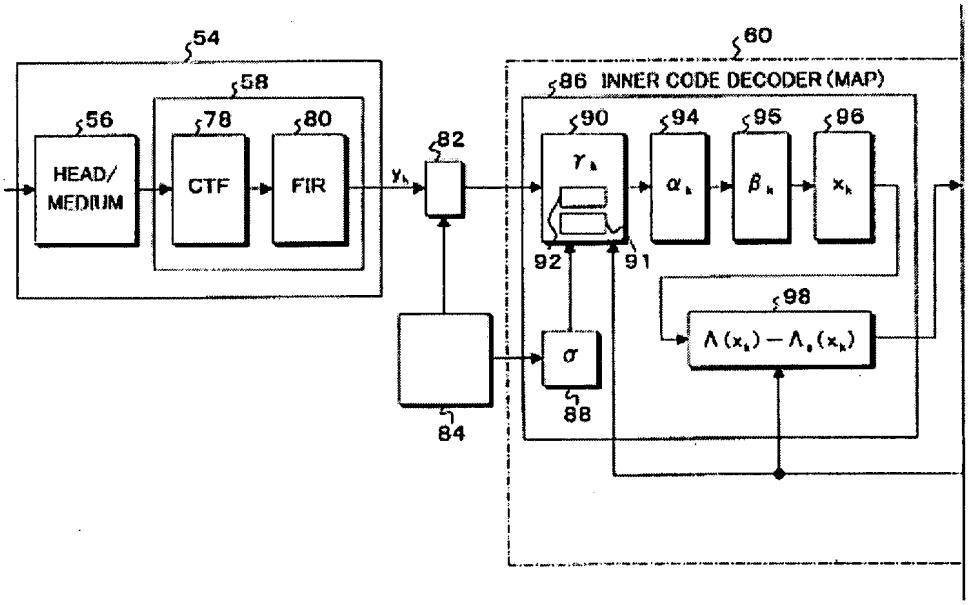
**1.** The abstract of the disclosure is objected to because said abstract is not descriptive. Correction is required.

### Claim Rejections - 35 USC § 102

**2.** **Claims 1-18** are rejected under 35 U.S.C. 102(e) as being anticipated by (US PGPub # 2003/0026028; FILED: October 29, 2001) **to Ichihara et al.** .

**As per Claims 1-18, Ichihara et al.** discloses, e.g., in para. 2, 13 et seq., and Figs. 4a, 10a, an equivalent tape drive system comprising tape head for tape access, filter means, signal decoders composed of viterbi processors and low density parity check decoders along with associated logic to generate read signals , process such to recover original data.

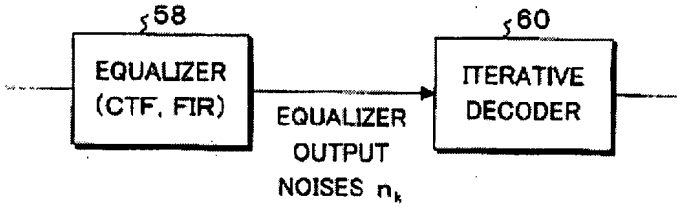
FIG. 4A




**As per Claim** 1, **Ichihara et al.** discloses, in para. 2, 13 et seq. and Figs. 4a, 10a, an equivalent system for use in a tape drive, the system comprising:

a tape head accessing a tape, the tape head generating read signals based on a spatial relationship between the tape head and the tape (e.g., in para. 2, 13 et seq.); a plurality of pulse shaping filters, each pulse shaping filter receiving the read signals and producing pulse-shaped signals, each pulse shaping filter having at least one filter parameter based on a possible tape head-to-tape spatial relationship, the at least one filter parameter unique to that filter (e.g., in para. 5 et seq., Fig. 4a:block 80, Fig. 10a);

FIG. 10A




and a signal decoder (e.g., in para. 5 et seq.) receiving the plurality of pulse-shaped signals and producing decoded output signals, the signal decoder comprising (a) a plurality of viterbi processors, each viterbi processor accepting pulse-shaped signals from one of the plurality of pulse shaping filters (e.g., in para. 6, 8, 17-18, 71 et seq.), and (b)

at least one low density parity check decoder producing the decoded output signals based on the output from one of the plurality of viterbi processors (e.g., in para. 6, 8, 17-18, 71 et seq.).

**As per Claim** 2, **Ichihara et al.** discloses, in para. 2, 13 et seq. and Figs. 4a, 10a, an equivalent system of claim 1 wherein each viterbi processor comprises a soft output viterbi processor (e.g., in para. 5-6, 8, 17-18, 71 et seq.).

**As per Claim** 3, **Ichihara et al.** discloses, in para. 2, 13 et seq. and Figs. 4a, 10a, an equivalent system of claim 1 wherein the at least one low density

parity check decoder is one low density parity check decoder having a low density parity check decoder input, the signal decoder further comprising decoder logic operative to select one of the plurality of viterbi processor outputs as the low density parity check decoder input(e.g., in para. 5-6, 8, 17-18, 71 et seq.).

**As per Claim** 4, **Ichihara et al.** discloses, in para. 2, 13 et seq. and Figs. 4a, 10a, an equivalent system of claim 1 wherein the at least one low density parity check decoder(e.g., in para. 5-6, 8, 17-18, 71 et seq.) is a plurality of low density parity check decoders, each low density parity check decoder having a low density parity check decoder input in communication with one of the plurality of viterbi processor outputs, the signal decoder further comprising decoder logic operative to select output from one of the plurality of low density parity check decoders as the decoded output signals.

**As per Claim** 5, **Ichihara et al.** discloses, in para. 2, 13 et seq. and Figs. 4a, 10a, an equivalent system of claim 1 wherein each viterbi processor generates a series of probabilities.

**As per Claim** 6, **Ichihara et al.** discloses, in para. 2, 13 et seq. and Figs. 4a, 10a, an equivalent system of claim 5 further comprising control logic(e.g., in para. 5-6, et seq.) selecting output from one of the plurality of viterbi processors.

**As per Claim** 7, **Ichihara et al.** discloses, in para. 2, 13 et seq. and Figs. 4a, 10a, an equivalent system of claim 6 wherein the control logic (e.g., in para. 37, 42, 71 et seq.) bases output selection on a distribution of the probabilities.

**As per Claim** 8, **Ichihara et al.** discloses, in para. 2, 13 et seq. and Figs. 4a, 10a, an equivalent system of claim 6 wherein the control logic (e.g., in para. 42, 71 et seq.) bases output selection on a standard deviation of the probabilities.

**As per Claim** 9, **Ichihara et al.** discloses, in para. 2, 13 et seq. and Figs. 4a, 10a, an equivalent system of claim 6 wherein each series of probabilities

contains at least one intermediate value and wherein the control logic bases output selection on at least one number of indeterminate values.

**As per Claim** 10, **Ichihara et al.** discloses, in para. 2, 13 et seq. and Figs. 4a, 10a, an equivalent system of claim 6 wherein the control logic(e.g., in para. 37, 42, 71 et seq.) bases output selection on at least one viterbi metric.

**As per Claim** 11, **Ichihara et al.** discloses, in para. 2, 13 et seq. and Figs. 4a, 10a, an equivalent method of retrieving data from tape comprising; reading the tape with a tape head to generate a read signal, the tape head having a spatial relationship with the tape as the tape passes the tape head, the spatial relationship described by at least one variable spatial parameter; filtering the read signal with a set of parallel filters, each filter receiving the read signal and producing a filtered signal, each filter based on at least one unique value for the at least one variable spatial parameter; processing each filtered signal with a viterbi algorithm; and generating a decoded output signal based on selecting and parity checking one of the viterbi processed filtered signals.

**As per Claim** 12, **Ichihara et al.** discloses, in para. 2, 13 et seq. and Figs. 4a, 10a, an equivalent method of claim 11 wherein generating a decoded output signal comprises:

selecting one of the viterbi (e.g., in para. 37, 42, 71 et seq.) processed filtered signals; and parity checking the selected viterbi processed filtered signals.

**As per Claim** 13, **Ichihara et al.** discloses, in para. 2, 13 et seq. and Figs. 4a, 10a, an equivalent method of claim 11 wherein generating a decoded output signal comprises:

low-density parity checking each of the viterbi(e.g., in para. 37, 42, 71 et seq.) processed filtered signals; and

selecting one of the low density parity checked viterbi processed filtered signals.

**As per Claim** 14, **Ichihara et al.** discloses, in para. 2, 13 et seq. and Figs. 4a, 10a, an equivalent method of

claim 11 wherein processing each filtered signal with a viterbi (e.g., in para. 37, 42, 71 et seq.) algorithm generates a series of probabilities.

**As per Claim** 15, **Ichihara et al.** discloses, in para. 2, 13 et seq. and Figs. 4a, 10a, an equivalent method of claim 14 wherein generating a decoded output is based on a distribution of the series of probabilities.

**As per Claim** 16, **Ichihara et al.** discloses, in para. 2, 13 et seq. and Figs. 4a, 10a, an equivalent method of claim 14 wherein generating a decoded output is based on standard deviation (e.g., in para. 37, 42, 71 et seq., Fig. 11) of the series of probabilities.

FIG. 11

| STATE | CORRELATION OF NOISES | | | | | | STANDARD DEVIATION OF NOISES |
|---|---|---|---|---|---|---|---|
| | $e_{-L}(S^n_k)$ | ... | $e_{-1}(S^n_k)$ | $e_0(S^n_k)$ | ... | $e_M(S^n_k)$ | $\sigma(S^n_k)$ |
| $S^n_2$ | $e_{-L}(S^n_0)$ | ... | $e_{-1}(S^n_2)$ | $e_0(S^n_0)$ | ... | $e_M(S^n_0)$ | $\sigma(S^n_0)$ |
| $S^n_1$ | $e_{-L}(S^n_1)$ | ... | $e_{-1}(S^n_1)$ | $e_0(S^n_1)$ | ... | $e_M(S^n_1)$ | $\sigma(S^n_1)$ |
| ..... | ..... | ... | ..... | ..... | ... | ..... | ..... |
| $S^n_{2^{L+Q+1}-2}$ | $e_{-L}(S^n_{2^{L+Q+1}-2})$ | ... | $e_{-1}(S^n_{2^{L+Q+1}-2})$ | $e_0(S^n_{2^{L+Q+1}-2})$ | ... | $e_M(S^n_{2^{L+Q+1}-2})$ | $\sigma(S^n_{2^{L+Q+1}-2})$ |
| $S^n_{2^{L+Q+1}-1}$ | $e_{-L}(S^n_{2^{L+Q+1}-1})$ | ... | $e_{-1}(S^n_{2^{L+Q+1}-1})$ | $e_0(S^n_{2^{L+Q+1}-1})$ | ... | $e_M(S^n_{2^{L+Q+1}-1})$ | $\sigma(S^n_{2^{L+Q+1}-1})$ |

**As per Claim** 17, **Ichihara et al.** discloses, in para. 2, 13 et seq. and Figs. 4a, 10a, an equivalent method of claim 14 wherein generating a decoded output is based on at least one number of indeterminate (e.g., in para. 37, 42, 71 et seq.) values in the series of probabilities.

**As per Claim** 18, **Ichihara et al.** discloses, in para. 2, 13 et seq. and Figs. 4a, 10a, an equivalent method of claim 14 wherein generating a decoded output is based on viterbi (e.g., in para. 37, 42, 71 et seq.) metrics.

## CONCLUSION

* Any response to this action should be mailed to:

Commissioner of Patents and Trademarks, Washington, D.C. 20231

**or faxed to:** (571) 273-8300 for all formal communications.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Guy J. Lamarre, P.E., whose telephone number is (571) 272-3826. The examiner can normally be reached on Monday to Friday from 9:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques, can be reached at (571) 272-6962.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-3609.

Information regarding the status of an application may also be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Guy J. Lamarre, P.E
Primary Examiner